Chapter 4

High Temperature Semiconductor Materials and Devices

By bringing quantum mechanics to evaluate the unit cells of various solids, Seitze initiated modern solid state physics. This study commenced with a series of papers under Wigner and Seitz. After Wigner got a Nobel Prize, he kept on telling the Nobel committee that the early series of ground breaking papers were really done by the young Seitz as his doctoral thesis, over mainly a period of two-years and had very little to do with himself the thesis advisor. But as Wigner put it, the Swedes simply would not listen to him. Since the first author already got a Nobel, not shared, Seitz as the second author, become the honor missed-out. There are many student/teacher won the Nobel prizes separately, but they were generally honored in very different topics or fields.

Introduction to Integrated Circuit (IC)

Computer chips are the engine of the modern information society. The nail-sized chips contain typically billions of transistors organized in the IC (integrated circuit). IC was pioneered by Jack Kelley of Texas Instruments (TI) and Bob Noyce of Intel. When Patrick Haggerty, the founder of TI, was seeking support for IC development, he told the head of Wright Patterson Air Force Base that it would "promote democracy", convinced the Air Force general to support TI and launched his IC development. Intel's computer in a chip concept has continued until this date, with Dr. Kelley winning a Nobel Price in physics in 2003, but Dr. Noyce, the oldest of the three founders of Intel, died before the Nobel honor could bestow on him. The chip business has reached $300 billions in 2007 or well over one trillion dollars if telecommunication equipments are included. All these hardwares and related softwares have been developed in the past few decades with a pace un-precedented in the development of any industry, and whose impact to all societies, particularly to the democratic trends, are most profound. Indeed, it is unique in the human history.

The technologies considered in this chapter could impact both the 1/3 trillion

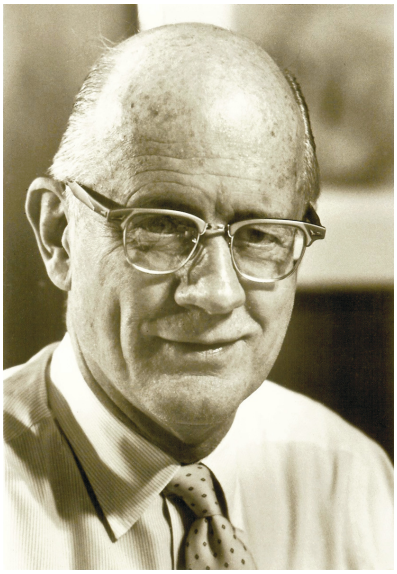
chip market and the $14 billion power devices. The state of the art technology developments have traditionally been led by the military, providing vital initial supports. But as the commercial chip performance marches forward relentlessly at an exponential rate, the military needs reduce to under 1% of the market and could often be met with commercial chips off-the-shelf. That is, except certain specialty devices for optoelectronics and for high temperature operations, the difference in military use and commercial use is disappearing. Efforts for specialty applications have mainly been the integration of thermal management for power operations and of optical functions.

As the design rule for computer chips marches forward from generation node to generation node, with each node of approximately 18 months where device density increases by a factor of two and speed increases also by a factor of two, giving rise to the resulting chip performance by a factor of four. Following Moore's law, chip performance has improved exponentially over the past four decades. While the device complexity in the chips has increased, the device dimensions have become much smaller, and the fabrication instruments have grown far more expensive. A typical fab line would now call for more than $2.5 billions to establish. Indeed, it has become an extremely capital-intensive endeavor. Amazingly, the industry has maintained, or even reduced the cost of fabricating the high-end chips. The fab cost of chips, for example, has reduced from one billion dollar per acre a decade ago to approximately the current $100M per acre. Part of this improvement is the use of ever larger wafers; from 150mm to 200mm to 300mm and soon to 400mm, all with virtually no cost increase in lithography per wafer and no reduction in the fabrication yield. These advances are based mostly on the enhanced throughput of processing instruments as measured by a reduced wafer processing time, which has been pushed competitively by the equipment vendors worldwide.

Superlattice Development at NanoDynamics-88, Inc.

NanoDynamics, Inc. was organized in 1988 to develop an X-ray microscope (Chap. 6). Raphael (Ray) Tsu called me in early 1993 and said that he had a most important invention in his life and wanted me to help develop it. Ray was instrumental in my joining the IBM Research Center, and after several decades, I still enjoy my discount rate in Hertz car rental that started the deep rental discount while I was at IBM Research. When asked about his invention, he said that it was the superlattice procedure applied to silicon. Ray and Leo Esaki are the fathers of the superlattice and quantum well development. This development was forbidden to continue by the IBM management in 1969 because they could not publish the concept in the harshly peer-reviewed Physical Reviews. But after

Esaki shared a Nobel Prize on the Esaki diode, which was the first award for IBM researchers, they were able to continue the superlattice development without the blessing of the management. In fact, almost all subsequent IBM work that resulted with Nobel Prizes were done without the blessing of its management. Superlattice has evolved into a mainstream in solid state materials, including an award of Nobel Price. I asked Ray to fax me his concept, and showed it to our chairman Dr. Fred Seitz, who initiated the phase space concept over the Wigner-Seitz cell and is generally considered the father of solid state. He was the Chairman of our small R and D Company, NanoDynamics-88, Inc.



Frederick Seitz

"Ray wants to construct layered silicon and non-silicon atoms epitaxially (following the same lattice pattern) for a heterojunction in silicon as a superlattice, what do you think?" I asked.

"This could be very important, if successful", Seitz answered.

"How shall we proceed?"

"If you want my opinion, don't talk about it." Seitz answered.

For academic endeavors, talking and giving seminars are 50% of the activities. We will be 50% lost, I thought.

"Also you don't write about it." Seitz continued.

Well, writing for publication is the other 50%. No writing? We will be totally lost, I thought. But Seitz added,

"File a patent application and try your best to verify it experimentally."

To file a patent is simple enough, but to demonstrate a new concept experimentally would require resources Nano did not have. At any rate, I did file a patent under Ray and the patent was allowed in a few months exactly as filed. I have never seen any patent application allowed as applied with absolutely no change or comment from the patent examiner. With an allowed disclosure, I sent the concept to *Nature*, which promptly accepted the write-up. With an issued patent and a *Nature* publication, I approached many trade journals and industry newsletters. They ALL endorsed the concept in their respective editorials, stating that it will be revolutionary if the silicon heterojunction could be successfully realized. These editorials probably would not be nearly as enthused without the *Nature* publication. I showed the pile of editorial endorsements to BMDO, which is a DoD agency, together with my solar wind isotope enrichment scheme (Chapter 3) and got two SBIR (small business innovation research) contracts, both with Phase I ($70,000 for the proof-of-concept phase) and Phase II ($750,000 for some developments). After three rounds of SBIRs and a few subcontracts as part of IPTs (integrated product team) from two large defense contractors, the silicon-based superlattice in materials and devices has been firmly established to warrant commercial scale manufacturing. A separate manufacturing entity, the C9 Corporation has been established under independent management and with the help of New York State. The C9 facility has begun to attract some serious attentions in the industry.

Silicon-based Superlattice Materials

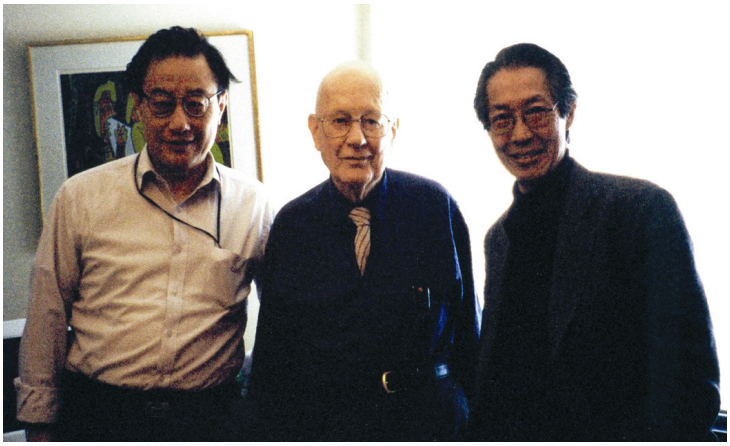
The superlattice and quantum well concepts were pioneered by Esaki and Tsu in 1969. They heard a seminar on silicon carbide (SiC) given by a scientist from the Westinghouse Corp. The seminar showed much promises and many material difficulties that it encouraged Esaki and Tsu to think that there must be a better way to develop this compound semiconductor, and proceeded to propose a stacking of layered compound semiconductor called superlattice. As Esaki had already made a prominent discovery on negative resistivity, the Esaki diode, their

first paper in 1969 centered also on the negative resistivity. Their paper, unfortunately, was rejected by Physical Reviews and other prominent journals and they were forced to publish it in IBM's own research journal with greatly reduced pronouncements. In fact, they also promised the IBM management to discontinue the superlattice work. Three decades later when Tsu and Esaki reviewed their extensive publications, they concluded that those articles got the highest praise by the referees were often the least referred to by others, while articles that encountered the most difficulties in getting accepted by the referees, such as their first superlattice article, were often the most important and consequently most cited by others. Comparing this to my own experience, for works within the "box", which implies as being conventional and providing incremental advances to the field, are easier for the referees to judge and appreciate. For works outside the "box", they are usually reviewed harshly by the referees and often get killed in the reviewing process. When one's work gets trashed harshly, it can easily reflect in one's own attitude toward reviewing other's work. That is, this "peer-review" system often brought out the worst competitive instincts from the follow scientists, famous or otherwise. To balance against such a killer instinct, it calls for a strong editor(s) of the peer-reviewed journals to bring some sensibility from the peer-scientists. Chandrasekhar, the premier astrophysicist and the editor in Ast Phys. Journal, for example, saved many of my calculations in neutron star material in spite of harsh criticisms from an equally prominent nuclear physicist. Without a strong editor in charge, those who adopt the peer-review system blindly and score their judgment without common sense could make the reviewing process completely arbitrary. This unfortunate adoption of mindless peer-reviewing includes prominent entities such as the National Science Foundation etc. who would often engage inexperienced scientists to do much of the tedious scoring without seasoned senior management in charge. NSF certainly does not have people like Chandra or Seitz in charge. A former director from DARPA of the Defense Dept, for example, wanted some of his program managers to assure a 15% or more failure rate, not higher success rate, in order to ensure the inclusion of more projects outside the "box", or "club", which are far more risky and could easily receive a poor score and be excluded. Such a demand did reduce a great many unnecessary and un-constructive comments, which are often the only comments routinely made in order to indicate that the reviewers were awake and could justify the per-diem charges.

Since Tsu and Esaki's 1969 superlattice article, there have been over fifteen thousand related articles and two thousand patents published. The compound semiconductor has mainly been GaAs, or the III-V (columns III and V of the periodic table) compounds. GaAs devices can out perform silicon devices by a

factor of ten. But every time certain GaAs devices found a market niche, and grew to one billion dollars or so, some engineers for silicon devices would find a silicon solution, such as making it smaller, to match the GaAs performance and produce it at much lower cost. Except for certain oscillators unique to the GaAs material and optical devices, silicon has consistently taken over the markets created by GaAs devices. Today, one dollar can purchase several billion transistors in a commodity silicon chip. This cost per transistor in silicon devices is many orders of magnitude below any other devices. Powerful as they are, however, silicon devices still cannot function at temperatures much beyond 100ºC or serve high power operations. The material of choice to deliver the high temperature, high power operations has been generally identified as silicon carbide (SiC), which can out perform silicon by a factor of 136. But SiC material is notoriously difficult to fabricate. As a result, when we (C9 Corporation) indicated that our Si/C superlattice would have the performance of SiC yet could be fabricated under the most powerful silicon processing technologies and produce devices almost at the cost of silicon, it does raise many eyebrows.

Our silicon-based superlattice procedure has applications on several fronts. The first front is the epitaxial insulator Si/O. Most silicon devices make use of a SiO_2 insulator, whose lattice dimension is 38% larger than silicon. SiO_2 built on silicon matrix must necessarily be amorphous and full of defects. Luckily Ed Ginston, formally at Bell Labs and a colleague of Ray Tsu at UNCC, found a capacitive way to measure the dangling bonds of the SiO_2/silicon interface because these loose bonds or defects would trap electrons and interfere with the transistor functions. Armed with a method to measure, it turned out that hydrogen would largely neutralize the dangling bonds in the interface. As a result, this “low defect” interface became the most vital component of the FET (field effect transistor) structure. Using Si/O superlattice, the inclusion of oxygen brought about almost no lattice mismatch, almost no strain, and in fact, delivers a defect density at the level of the best Si/SiO_2 interface annealed with hydrogen. This low defect epi-insulator brings about many new device possibilities and it is the heart of our new silicon-based superlattice structure, with a few particular applications listed below.



Dr. Seitz, Dr. Tsu and author

Si/O Superlattice and SOI Wafers

Amount the initial superlattice applications is the SOI wafers. First supported by the Air Force to reduce the ionizing radiation effect to the chips, SOI (silicon on insulator) wafers have become a high–end commodity item for chip fabrications. By constructing the ultra-thin chip material on an insulating layer, which will not generate noise from the ionizing radiation, the not too thin layer of the semiconductor material in early days would allow the transistors to have a greatly reduced cross section to intercept the ionizing radiation, mostly from outer space. More importantly, having the insulating layer beneath the device would greatly reduce the device cross-talk. As a result, the devices using SOI wafers can be placed much closer and with reduced need of guard rings etc.

There are two basic technologies for making SOI wafers. The first method historically is ion implantation. Oxygen ions under acceleration would penetrate through the wafer surface and form SiO_2 beneath the surface. But in so doing, the top layer for the device construction becomes totally cracked up and cannot be nursed (annealed) back into the proper crystalline matrix. An IBM patent called for implanting the ions at an elevated temperature which greatly reduces the damage from ion implantation. But some other difficulties, such as the bell-shaped penetration depth, the non-uniformity over the entire wafer surface, particularly for the large wafer sizes, as well as the high cost of the implanting instrument and its relatively low throughput, have greatly reduced the appeal of this procedure in the industry.

The second method is the bonded wafer approach that a wafer with oxide surface is bonded to a second wafer without oxide and shave the second one to a desired thickness. This approach is made famous by the Soitec Corporation of France, which has been backed by the French government. The Soitec method uses two wafers A and B. They first oxidized the A surface to form amorphous SiO_2 and pressed B onto the oxided A surface. They then applied a "smart cut" on B by shooting protons from the B surface and anneal. As protons become hydrogen, they would crack the surface of B into two parts, with the non-impacted B surface remaining attached to A while the portion of B damaged by the protons can then be mechanically smoothed and used as a subsequent A wafer for another oxide surface. The thin layer of B attaching on A is first mechanical smoothed by large machines at low cost. Now comes the difficult part, the ultra-thinning process. An Xerox sheet of paper is approximately 75 micrometer (μ) thick. The B surface after the "smart-cut" can readily be thinned from over 100μ to a few μ. But to thin the remaining thin surface by another 90% or more, with an accuracy of say 2% of the wavelength of light, or 0.01μ, becomes extremely difficult and expensive. Soitec uses chemical-mechanical-polishing (rubbing gently with a mild acid) and monitors the depth with an ellipsometer (laser interferometer) mm by mm over an entire wafer surface which becomes truly a messy tech, and the situation will get worse as the top device layers must becomes thinner in future generations. One can use electron microscopes or some other means to measure the surface at every micron and reach some exact thickness everywhere on a wafer surface, but in so doing, the SOI wafers can no longer be a commodity product.

By using Si/O superlattice, the insulating Si/O region is grown epitaxially on silicon, which can be followed by growing the ultra-thin silicon layer epitaxially on Si/O without shaving and monitoring at high cost. As a result, the SOI wafers can be grown as thin or as thick as the device designers call for. Using SOI wafers to fabricate high-end chips, it would incur an extra cost of one thousand dollars or so for the 300 mm wafers. While IBM and AMD have utilized the SOI advantages, Intel has largely resisted its use, claiming that the quality of the SOI top depleted layers has not met their specifications. If the SOI were fabricated under the Si/O superlattice procedure, or as we call it the SOeI (semiconductor on epi-insulator) wafers, the top layer in Si or the wide bandgap Si/C could readily meet the parameters of the current 45 nm node as well as 32 nm and 22 nm nodes in a few years because the thinner the top layer, the easier to fabricate under our superlattice procedure. Indeed SOeI wafers have some advantages such as having a wide bandgap material for high temperature, high power devices, but the wafer supply is essentially a commodity business, a messy tech,

that calls for large capital and strong management. Note that Soitec of France has been in the SOI business for over two decades and only in 2005 did they make a profit. Another simple tech approach to use the silicon-based superlattice is to construct Si/O for the gate dielectric stack for the CMOS.

High Gate Dielectric and Low Interconnect Dielectric for FET Devices

Most of the chip devices, perhaps 85%, are based on the CMOS where a n-type MOSFET couples with a p-type MOSFET, with the n-type for on-function and the p-type for off-function. The gates of the CMOS for the current 45 nm node is SiO_2 at only one nm thick, or two molecular layers. Because this dielectric layer is so thin that electrons can easily tunnel with moderate bias, it is now responsible for ~ 60% of the power loss of the transistors. A thicker gate with less leakage current would reduce the gate capacitance, whose induced charges provide the transistor charge transport at the channel beneath. One solution to this difficulty is to increase the dielectric constant of the gate material so that a thicker gate would retain the same capacitance to provide the charge transport. Intel scientists have successfully inserted some Hafnium dioxide into the gate oxide and Dr. Moore, co-founder of Intel, called it the most important advance in chip technology in the past 4 decades. To insert foreign elements into the low defect SiO_2/Si interface is indeed very challenging, but to incorporate foreign elements to our Si/O insulating superlattice fabricated on silicon is relatively simple. In fact, because the oxygen atoms are already present in the layered surface at the desired lattice position, elements of almost the entire periodic table, including many metal oxides to be systematically incorporated into the gate stack under the superlattice procedure. This is perhaps the most attractive "simple tech" using the Si/O superlattice structure in addition to the formation of SOeI wafers.

While the gate stack for FET calls for high dielectric Ķ for high capacitive charges, the interconnect calls for low dielectric Ķ for low capacitance and low time delay in the signal transmission. Using the epi-Si/O structure, both the high Ķ or low Ķ can be woven into the superlattice fabrication process. Note that as the complexity of chips increases, the limiting speed or bottleneck can arrive from the gate stack in materials as well as from the device interconnect designs in practical circuits. There are limits as to how many layers of interconnect can practically be incorporated in an IC, and therefore the low Ķ dielectric could be as important as the high Ķ dielectric.

Silicon Carbon Lamella Si/C

The third silicon-based superlattice material is the silicon carbon lamella (Si/C). There is no natural SiC except for those obtained from meteorites, which is colorless. All man-made SiC is black with graphite contamination. Carbon bond (σ bond) in the graphite structure is stronger than that in diamond or in SiC. Therefore once formed, the graphite structure is irreversible under nominal pressure. The recent interest in carbon nanotube material is really carbons formed with wrapped around graphite bonds, and therefore they are very stable. SiC devices can potentially function 136 times better than silicon devices with respect to higher operating temperatures, higher power, faster speeds, etc. (GaAs is ten times that of silicon) But even after the Defense Department has spent more than $2.4 billion in R and D, the higher material performance remains mostly a dream. The key reasons include, SiC does not have a liquid phase and cannot be made into a single crystal like silicon. To form a binary material for a crystal structure, both elements C and Si must migrate into a proper lattice position in order to reach a low energy state and stay there as a stable lattice structure. But carbon has much higher binding energy than silicon and will not migrate at temperatures much below 1,600˚C, which is higher than silicon's melting point of 1,414˚C and would generate substantial vapor pressure. This silicon vapor creates small voids or micro-pipes as the vapor collapses. Note that without carbon atoms migrating, defects of SiC matrix cannot be annealed or reduced at any temperature beneath 1,600˚C. Worse yet, SiC can form a great variety of crystal structures, with each a different lattice dimension and coefficient of thermal expansion. These crystal forms would all participate in some equilibrium fraction at an elevated fabrication temperature, but at low operating temperature where the device must function, the crystal lattice of mixed structures retains a great deal of localized strain. Devices made from such a material with highly localized strain would often fail as soon as they are turned on as the strains are released.

Under the silicon-based superlattice procedure, the carbon and silicon precursor molecules can be woven with the dopant-containing precursor molecules layer-by-layer in the Si/O structure uniformly under conventional silicon processing environment. We have therefore altered the SiC fabrication from an impossible messy tech to a clean simple tech under the silicon-based superlattice routine. Starting from an inexpensive silicon substrate as template, we construct a Si/O epitaxial (crystalogically aligned) insulator. The Si/O insulator can reach thousands of atomic layers with virtually no strain or structure degradation. It can also incorporate Si/C superlattice with some strain and with the Si/O in the midst of Si/C matrix.

GaN Constructed on Si/C

Gallium Nitride (GaN) is a semiconductor with a larger bandgap than SiC and can be fabricated with a lower thermal budget than that for SiC. GaN can deliver LEDs with "cool green" spectrum at a high efficiency of 50% and high brightness, and the GaN-based LEDs have reached a market size of ~$4billion, with 90% of the GaN material fabricated on sapphire substrate and under 10% fabricated on SiC substrate. Sapphire (Al_2O_3) has poor thermal conductivity that limits the power density for the GaN devices built upon. Sapphire is an insulator, which must be removed if the GaN device adopts a vertical design for high current transport. SiC is a semiconductor with high thermal conductivity, which can support the vertical current transport as well as being the substrate template for GaN growth. But SiC is a well known expensive and defective material, which renders the GaN devices to be costly, at small sizes and with low yield. Cree's GaN using SiC substrate has reached $600 millions in sales, but reduced to $400 millions in recent years because of its high prices. LEDs using SiC remain to be a dominant business in Cree' products.

Using Si/C as substrate to construct GaN, the template substrate can be rather thin, that is, at low cost, while using the thick silicon material to provide the mechanical support as well as providing the current source, so that high quality GaN material can be grown with this buffer arrangement to avoid lattice mismatch, and grown under conventional CVD for GaN at a rate of several microns per hour with very high yield.

Graphene

Si/C lamella is fabricated with a carbon-containing precursor molecule on a silicon substrate template. One of the carbon-containing molecules is simply the carbon monoxide CO, which has very high sticking coefficient to adhere onto almost any surfaces; metal, semiconductor, or insulator. The Si/CO superlattice shows a direct bandgap under photoluminescence at 2.3eV. The Si/CO lattice matrix, on the other hand, can be constructed at a slightly elevated temperature to isolate the carbon layer with the discharge of CO_2 under vacuum. Such a monolayer of carbon constructed on an appropriate substrate template can also produce an ultra-thin honeycone graphite structure or graphene, which has attracted much recent academic and industrial attentions. The two dimensional graphene has zero bandgap and provides massless pure Dirac fermions with ballistic mobility and has a structure stronger than any known material because of its perfect lattice structure without defects. Interesting as it may be, graphene however is not a conventional semiconductor material and we shall refrain from

going into the subject matter too much except that the production of graphene could probably be derived from the high throughput procedure of our superalttice fabrication.

The sixth application of the wide bandgap silicon superlattice is for high temperature solar cells. The subject matter involves, however, issues such as economics, history, geology, etc. that are not obvious from a purely technical point of view. These related important issues will be addressed in a separate chapter, the Chapter 5 below.

Epitaxial All the Way and the Fabrication Equipment

On the Si/O insulator, we can either deposit an ultra-thin silicon layer for the ultra-thin SOI wafers, or an Si/C lamella for the SOeI (semiconductor on epi-insulator) wafers upon which high temperature, high power devices in chips or single devices can be constructed. In this epi-construction routine, dopants in both p and n type can be woven lamellaly, allowing p and n to be alternately positioned in ultra-thin layers; allowing high dielectric materials as mentioned earlier to be woven with the gate insulating stack where the current leakage has become a major concern of power loss in the CMOS, or low dielectric material for the interconnects linking the devices to be arranged vertically for 3-dimensional architectures. In short, the notion of epitaxial all the way would certainly create a great many new design possibilities. The silicon-based superlattice procedure is therefore a breakthrough "simple tech". It will probably evolve into a "messy tech" again as it gains popularity and is adopted as an industry standard.

For commercial use, we have designed a high throughput fabrication instrument for superlattice fabrication in order to be useful to the semiconductor industry. The fabrication instrument is a modified atomic layer deposition (ALD), which is conventionally also "messy tech" equipment. ALD is designed to incorporate the delicate deposition procedure of MBE (molecular beam epitaxy) so that at extremely high vacuum, the slow deposition process would allow a great variety of precise processing control with a relatively fast processing speed of CVD (chemical vapor deposition). MBEs are typically used as research tools while CVDs are industry production tools. By combining the functions of MBE with the throughput of CVD, ALD becomes truly a messy tech tool almost by definition. For C9 Corporation, our modification of the ALD instrument has taken advantage of self-limiting surface chemistry function specific to the superlattice fabrication procedure so that the processing instrument

becomes a “simple tech” with very high throughput under precise and exact deposition steps. The Si/C lamella wafers and devices become therefore our first line of products under the management of the C9 Corporation.

CHAPTER FOUR REFERENCES

On the Superlattice Si/O

R. Tsu, Chapter 6 of “Superlattice to Nanoelectronics”, Elsevier, Publisher.